

DERWENT-ACC-NO: 2000-474789

DERWENT-WEEK: 200041

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TITLE: Self-aligned copper structure
formation in integrated circuit manufacture, involves
depositing copper selectively and electrochemically in
trench and planarizing copper, insulating seed
and barrier layers

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PRIORITY-DATA: 1999US-0387436 (September 1, 1999)

PATENT-FAMILY:

PUB-NO

PUB-DATE

LANGUAGE

PAGES

MAIN-IPC

US 6080656 A

June 27, 2000

N/A

006

H01L 021/4763

APPLICATION-DATA:

PUB-NO

APPL-DESCRIPTOR

APPL-NO

APPL-DATE

US 6080656A

N/A

1999US-0387436

September 1, 1999

INT-CL (IPC): H01L021/44, H01L021/4763

ABSTRACTED-PUB-NO: US 6080656A

BASIC-ABSTRACT:

NOVELTY - Barrier layer (18), seed layer (20) and
insulating layer are formed
sequentially over dielectric trench layer (12) on
semiconductor structure (11).

Insulating layer is patterned to expose seed layer on bottom and side walls of trench (30). Then, copper (50) is deposited selectively and electrochemically in trench and copper, insulating, seed and barrier layers are planarized stopping at dielectric layer.

DETAILED DESCRIPTION - The barrier layer (18) comprises tantalum nitride having a thickness of between about 50-600 Angstrom and seed layer (20) comprised of physical vapor deposited copper having thickness between 1000-3000 Angstrom .

USE - In integrated circuit manufacture used in memories, microprocessor and micro computers.

ADVANTAGE - Because of the self-aligned copper geometry, the copper suffers reduced dishing. Copper lines and interconnects with reduced dishing provides improved RS uniformity and improved planarization needed to form the multilevel metallisation demanded for current devices.

DESCRIPTION OF DRAWING(S) - The figure shows sequential sectional view explaining the process of forming copper structure.

Semiconductor structure 11

Dielectric trench layer 12

Barrier layer 18

Seed layer 20

Trench 30

Copper 50

CHOSEN-DRAWING: Dwg.6/6

TITLE-TERMS: SELF ALIGN COPPER STRUCTURE FORMATION
INTEGRATE CIRCUIT
MANUFACTURE DEPOSIT COPPER SELECT